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2. (amended) The driver circuit as claimed in claim 1, wherein the at least one input node for the input signal is connected to the at least one sub-driver.

A1 cont.

3. (amended) The driver circuit as claimed in claim 2, wherein the at least one input node for the input signal is connected to the at least one evaluation circuit.

4. (amended) The driver circuit as claimed in claim 1, wherein two or more sub-drivers and two or more evaluation circuits are provided, each sub-driver being connected to an evaluation circuit.

B

5. (amended) The driver circuit as claimed in claim 4, wherein two or more feedback capacitors are provided, each feedback capacitor being provided between an output node of the driver circuit and an input node of an evaluation circuit.

6. (amended) The driver circuit as claimed in claim 1, wherein the input node(s) of the evaluation circuit(s) is/are at low impedance.

7. (amended) The driver circuit as claimed in claim 1, wherein the at least one sub-driver has one or more transistors.

8. (amended) The driver circuit as claimed in claim 1, wherein at least one control transistor is provided in the at least one sub-driver, said transistor being respectively connected to an evaluation circuit.

9. (amended) The driver circuit as claimed in claim 1, wherein the at least one feedback capacitor is designed as a linear capacitor.

a1 cont.

10. (amended) The driver circuit as claimed in claim 1, wherein the at least one feedback capacitor is designed as a nonlinear capacitor.

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11. (amended) The driver circuit as claimed in claim 10, wherein the nonlinear capacitor is formed from at least one PMOS transistor and/or at least one NMOS transistor.

B

12. (amended) A method for operating a driver circuit as claimed in claim 1, wherein a low-harmonics current is generated in the driver circuit and supplied to a load, and wherein an edge steepness that is independent of the present load situation is set in the driver circuit.

a2

14. (amended) The method as claimed in 12 wherein, in order to set the load-independent edge steepness, the output characteristic of the driver circuit is measured by the feedback circuit and evaluated therein, and wherein the drive strength of the at least one sub-driver is regulated on the basis of the evaluation results.

a3

16. (amended) The use of a driver circuit as claimed in claim 1 of a method as claimed in claim 12 for improving the electromagnetic compatibility of electronic components, in particular of integrated circuits.

In the Claims

1. (amended) A driver circuit, having at least one input node [(11)] for an input signal and at least one output node [(12)] for an output signal, having one or more, preferably two, sub-drivers [(20, 30)] and having a feedback circuit [(40)], which has one or more evaluation circuits [(50, 60)] and one or more feedback capacitors [(41, 42)], the evaluation circuit(s) [(50, 60)] being connected to the sub-driver(s) [(20, 30)] and the feedback capacitor(s) [(41, 42)] respectively being provided between an output node [(12)] of the driver circuit [(10)] and an input node [(51, 61)] of an evaluation circuit [(50, 60)], the at least one evaluation circuit [(50, 60)] having a first inverter stage [(53, 54)], coupled to the input node [(51, 61)] of the evaluation circuit [(50, 60)], and also a second inverter stage [(56, 57)], connected in series with the first inverter stage [(53, 54)], the first inverter stage [(53, 54)] being short-circuited with the input node [(51, 61)].

2. (amended) The driver circuit as claimed in claim 1, wherein the at least one input node [(11)] for the input signal is connected to the at least one sub-driver [(20, 30)].

3. (amended) The driver circuit as claimed in claim [1 or] 2, wherein the at least one input node [(11)] for the input signal is connected to the at least one evaluation circuit [(50, 60)].

4. (amended) The driver circuit as claimed in [one of] claim[s] 1 [to 3], wherein two or more sub-drivers [(20, 30)] and two or more evaluation circuits [(50, 60)] are provided, each sub-driver [(20, 30)] being connected to an evaluation circuit [(50, 60)].

5. (amended) The driver circuit as claimed in claim 4, wherein two or more feedback capacitors [(41, 42)] are provided, each feedback capacitor [(41, 42)] being provided between an output node [(12)] of the driver circuit [(10)] and an input node [(51, 61)] of an evaluation circuit [(50, 60)].

6. (amended) The driver circuit as claimed in [one of] claim[s] 1 [to 5], wherein the input node(s) [(51, 61)] of the evaluation circuit(s) [(50, 60)] is/are at low impedance.

7. (amended) The driver circuit as claimed in [one of] claim[s] 1 [to 6], wherein the at least one sub-driver [(20; 30)] has one or more transistors [(21, 22, 23; 31, 32, 33)].

8. (amended) The driver circuit as claimed in [one of] claim[s] 1 [to 7], wherein at least one control transistor [(24, 34)] is provided in the at least one sub-driver [(20, 30)], said transistor being respectively connected to an evaluation circuit [(50; 60)].

9. (amended) The driver circuit as claimed in [one of] claim[s] 1 [to 8], wherein the at least one feedback capacitor [(41, 42)] is designed as a linear capacitor.

10. (amended) The driver circuit as claimed in [one of] claim[s] 1 [to 9], wherein the at least one feedback capacitor [(41, 42)] is designed as a nonlinear capacitor.

11. (amended) The driver circuit as claimed in claim 10, wherein the nonlinear capacitor is formed from at least one PMOS transistor [(43)] and/or at least one NMOS transistor [(44)].

12. (amended) A method for operating a driver circuit as claimed in [one of] claim[s] 1 [to 11], wherein a low-harmonics current is generated in the driver circuit and supplied to a load, and wherein an edge steepness that is independent of the present load situation is set in the driver circuit.

14. (amended) The method as claimed in 12 [or 13,] wherein, in order to set the load-independent edge steepness, the output characteristic of the driver circuit is measured by the feedback circuit and evaluated therein, and wherein the drive strength of the at least one sub-driver is regulated on the basis of the evaluation results.

16. (amended) The use of a driver circuit as claimed in [one of] claim[s] 1 [to 11 and/or] of a method as claimed in [one of] claim[s] 12 [to 15] for improving the electromagnetic compatibility of electronic components, in particular of integrated circuits.